# Implementation and Algorithms for the FPD DSM Tree High-tower(actually high-tube :-) version

Falk Meissner

February 3, 2004

Description: The first layer of DSM boards places three tresholds on each single PMT. These thresholds are SIZEORDERED $th0 < th1 < th2$. The thresholds are the same for all PMTs. A register selects which of the three thresholds is used to trigger STAR, if any of the PMTs is above it. The three thresholds are coded into two bits indvidually for each module and these 8*2 bits are available in the scaler boards.
Find a drawing of the FPD-DSM tree at
http://www.star.bnl.gov/STAR/html/fpd_l/fy03/electronics/index.html

## 1 FPD-layer0, FPD-FE/W-001, 002, 003, 005, 006, 007, 008, 009, 010, 011

This Algorithm places thresholds on all 16 8bit input channels. Unused channels need to be zeroed out in the LUTs. These thresholds are size ordered $th0 < th1 < th2$. An 'or' is build for each threshold, from all the PMTs in each board. The tree threshold bits are propagated to the next layer. This DSM algorithm also contains the **HALT-COUNTER** mechanics.

Input: up to 16x8bit ADC values

Registers: R0: FPD-PMT-th0 (8)
R1: FPD-PMT-th1 (8)
R2: FPD-PMT-th2 (8)
R3-R12 dummies
R13-15 Haltcounter mechanics

LUT: Pedestal subtraction/ masking unused channels

1st. Clock: Place three thresholds on each 8bit ADC channel

2nd Clock: Combine all channels into one bit per threshold. Bit is set ('1') if any PMT is above the specific threshold

Output (0-2) th-bits 0-2, (3-15) empty

## 2 FPD-layer0, FPD-FE/W-004

Same functionality as FP001. This is the split module. Only the channels 0-6 and 7-13 are used.

Input: 2x7 8bit ADC values; split module
Assignment of North and South is swaped for East and West crate
ch0-6 East-North; West-South
ch7-13 East-South; West-North

Registers: R0-R2 same as FP001, no halt counter.

LUT: same as FP001

1st. Clock: same as FP001

2nd Clock: same as FP001

Output (2 cables)
Lower bits East-North; West-South; ch0-6
(0-2) th-bits 0-2, (3-15) empty
Upper bits East-South; West-South, ch7-13
(16-18) th-bits 0-2, (19-31) empty

## 3 FPD-layer1, FPD-FE/W-101, North-South modules

combine 8x 3bits to the high-tube threshold bits of a detector module.

Input: 8xthreshold bits ch0-3 E-N/W-S and ch4-7 E-S/W-N

Registers: None

LUT: 1:1

1st. Clock: Combine Bits

2nd Clock: Delay

Output (2 cables)
Lower bits East-North; West-South
(0-2) Threshold Bits, (3-15) empty
Upper bits East-South; West-South
(16-18) Threshold Bits, (19-31) empty

## 4 FPD-layer1, FPD-FE/W-102, Top/Bottom

Same functionality as FP101, only the first 4 channels are used from the top/bottom modules.

Input: 4*3 threshold bits ch0-1 Top; ch2-3 Bottom

Registers: None

LUT: 1:1

1st. Clock: Combine Bits

2nd Clock: Delay output

Output (2 cables)
Lower bits Top
(0-2) ADC sum, (3-15) empty
Upper bits Bottom
(16-18) ADC sum, (19-31) empty

## 5 FPD-layer2, L1-FP201

Code the three threshold bits into two bit numbers for the use in the scalerboards. A registers selects which threshold is used to trigger STAR.

Input: One Set of threshold bits per detector module
ch0: East-North
ch1: East-South
ch2: East-Top
ch3: East-Botton
ch4: West-South
ch5: West-North
ch6: West-Top
ch7: West-Botton

Registers: L1: index:11
The registers R0-R2 are left for combatibility. They do not have any effect in the high-tower version.
R0: ADC-threshold-0 (unused)
R1: ADC-threshold-1 (unused)
R2: ADC-threshold-2 (unused)
R3: FPD-trigger-threshold-select: '0'-th0; '1'-th1; '2'-th2; '3'-off

LUT: 1:1

1st. Clock: Delay

2nd Clock: Code threshold comparision into scaler bits seperately for all 8 modules. Two bits per module: '00'-ADC<th0, '01'-ADC>th0, '10'-ADC>th1, '11'-ADC>th2. STAR fpd trigger fires if any module is above threshold as selected by R3.

Output (2 cables)
Lower bits to last DSM 301
(0) FPD-trigger East
(1) FPD-trigger West
(2-15) empty
Upper bits to FPD scaler, see below

## 6 FPD asymmetry scaler

| Bit | Name | From DSM | JP6 Bit |
|---|---|---|---|
| 1 | BBC TAC-Window 0 | VT201 | 0 |
| 2 | FPD-NE-thbit0 | FP201 | 0 |
| 3 | FPD-NE-thbit1 | FP201 | 1 |
| 4 | FPD-SE-thbit0 | FP201 | 2 |
| 5 | FPD-SE-thbit1 | FP201 | 3 |
| 6 | FPD-TE-thbit0 | FP201 | 4 |
| 7 | FPD-TE-thbit1 | FP201 | 5 |
| 8 | FPD-BE-thbit0 | FP201 | 6 |
| 9 | FPD-BE-thbit1 | FP201 | 7 |
| 10 | FPD-SW-thbit0 | FP201 | 8 |
| 11 | FPD-SW-thbit1 | FP201 | 9 |
| 12 | FPD-NW-thbit0 | FP201 | 10 |
| 13 | FPD-NW-thbit1 | FP201 | 11 |
| 13 | FPD-TW-thbit0 | FP201 | 12 |
| 14 | FPD-TW-thbit1 | FP201 | 13 |
| 15 | FPD-BW-thbit0 | FP201 | 14 |
| 16 | FPD-BW-thbit1 | FP201 | 15 |
| 17 | CTB multi>N | LD301 | 1 |
| 18-24 | bunch id | | |